24) **math coprocessor structure and operation**

**Math Coprocessor Operation**

- Shares the same Data, Address and Control BUS as the main processor

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

OFFSET 15…0

SELECTOR

P DPL 0 TIP 000 no. words

OFFSET 31…16

7

- Two different chips for old processors

- On the same silicon die starting with 486DX

**- Instructions preceded by an ESC sequence-anunta procesoru principal ca nu sunt pt ele**

-Operates in parallel with main processor

- Coprocessor may overtake BUS for longer periods if more data is needed

- Coprocessor has no access to registers but can use registers for addressing

- All addressing modes are available except immediate addressing

- Uses special synchronization signals to cooperate

- Instructions take tens to hundreds of cycles to complete

**Math Coprocessor Structure**

- Register Stack

- Control Register

- Status Register

- Tag Register

- Instruction Pointer

- Data Pointer

-unitate de executie

-unitate de control

-unitate de comanda

Exista un semnal de busy (sincronizare) -> spune daca coprocesorul mathematic lucreaza sau nu.